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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,480	07/29/2003	Roberto Fabian Averbuj	030198	9692

7590 09/11/2007

QUALCOMM Incorporated
Attn: Patent Department
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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,480	AVERBUJ ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,22-29,32,34-36 and 38* is/are rejected.

7)☒ Claim(s) *4-21,30,31,33 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/23/07*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *8/31/07* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on February 28, 2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney, or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3, 22, 24-25, 26-29, 32, and 34-36 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 10-11, and 15-17 of U.S. Patent No. 7,184,915. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 1 of the present application is substantially the same as claims 1 and 3 of the U.S. Patent as shown below:

Claim 1 of the present application recites: "A system comprising: a centralized built-in self-test (BIST) controller that stores an algorithm for testing a plurality of memory modules, wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol; and a plurality of distributed sequencers that interpret the commands based on the command protocol and apply the generalized commands to the memory modules, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains."

Claim 1 of the U.S. Patent states: "A system comprising: a plurality of memory modules, at least one memory module having a clock domain different that other of said plurality of memory modules; a single built-in self-test (BIST) controller that stores an algorithm for testing the memory modules; and a plurality of sequencers, each

sequencer coupled to a different subset of the memory modules, wherein each subset of the memory modules is selected to include the memory modules having common clock domains, and each sequencer controls the application of the test algorithm to the respective subset of memory modules in accordance with the common clock domain of that subset of memory modules."

Claim 3 of the U.S. Patent states: "3. The system of claim 1, wherein the sequencer comprises: a plurality of command controllers that implement the commands in accordance with a command protocol; and a command parser to parse each command to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller. "

Claim 10 of the U.S. Patent claims "The system of claim 1, wherein the memory interface comprises a data generation unit that receives data signals from the sequencer and generates transformed data signals based on the data signals and the physical characteristics of the memory module." (claim 26 is the only independent t claim that requires the limitations of claim 10 of the US Patent)*

The U.S. Patent claims a 'single' BIST while the present application recites a 'centralized' BIST. However, the 'single' BIST performs the same function as the 'centralized' BIST. Therefore, one is merely an obvious variation of the other.

The U.S. Patent claims 'a plurality of sequencers, each sequencer coupled to a different subset of the memory modules' while the present application recites 'a plurality of distributed sequencers'. These also perform the same function and are simply obvious variations in the wording.

Claim 26 of the present application recites "A device comprising: centralized built-in self-test (BIST) control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of distributed memory modules having different timing requirements and physical characteristics; and distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements and physical characteristics of the memory modules, said distributed means including a plurality of sequencers, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains." *

Claim 28 of the present application recites "A method comprising: directing application of an algorithm from a centralized built-in self-test (BIST) controller by issuing generalized commands that conform to a command protocol to test a plurality of memory modules; and interpreting the commands with a distributed set of sequencers to apply the commands as one or more sequences of memory operations in accordance with the command protocol, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains."

As can be seen above the remaining independent claims also contain the limitations of the U.S. Patent claims stated above and are therefore rejected for the same reasons.

Claim 2 of the present application recites "The system of claim 1, wherein the generalized commands specify the algorithm in accordance with the command protocol and without regard to timing requirements of the memory modules. This limitation is covered in claim 15 of the U.S. Patent, which requires in part "the commands conform to a generalized command protocol that substantially defines the test algorithm without regard to physical characteristics and timing requirements of the memory module."

Claim 3 of the present application recites "The system of claim 1, wherein the generalized commands specify the algorithm without regard to physical characteristics of the memory modules." This limitation is also covered in claim 15 cited above.

Claim 22 of the present application recites the following: "The system of claim 1, further comprising a plurality of memory interfaces coupled between the sequencers and the memory modules, wherein the memory interfaces apply the commands to the memory modules under the direction of the sequencers and in accordance with physical characteristics of the memory module." These limitations are covered in claim 10 of the U.S. Patent, which claims "The system of claim 1, wherein the memory interface comprises a data generation unit that receives data signals from the sequencer and generates transformed data signals based on the data signals and the physical characteristics of the memory module."

Claim 24 of the present application recites the following:" The system of claim 1, wherein the sequencers apply the commands to the respective memory modules in accordance with timing requirements of the memory modules." These limitations are covered in claim 2 of the U.S. Patent, which claims "The system of claim 1, wherein the sequencer controls an application speed of the memory operations to the memory interface in accordance with timing requirements of the memory module."

Claim 25 of the present application recites the following:" The system of claim 1, wherein each of the sequencers comprises: a plurality of command controllers that implement the commands in accordance with a command protocol; and a command parser to parse each of the commands to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller." These limitations are covered in claim 2 of the U.S. Patent, which claims "The system of claim 1, wherein the sequencer comprises: a plurality of command controllers that implement the commands in accordance with a command protocol; and a command parser to parse each command to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller."

Claim 27 of the present application recites the following: "The device of claim 26, wherein the distributed means includes interface means for generating translated address and data signals based on the physical characteristics of the memory modules

to apply the BIST algorithm to the memory modules." These limitations are covered in claims 10 and 11 of the U.S. Patent, which claim: 10. "The system of claim 1, wherein the memory interface comprises a data generation unit that receives data signals from the sequencer and generates transformed data signals based on the data signals and the physical characteristics of the memory module." And 11. "The system of claim 10, wherein, in response to a control signal received from the sequencer, the data generation unit automatically transforms the data to store inverted data within at least one of neighboring rows, neighboring columns, and neighboring row-column matrices of the memory module."

Claim 29 of the present application recites the following:" The method of claim 28, wherein the generalized commands specify the algorithm without regard to physical characteristics and timing requirements of the memory modules." These limitations are covered in claim 15 of the U.S. Patent, which claims "The system of claim 1, wherein the commands conform to a generalized command protocol that substantially defines the test algorithm without regard to physical characteristics and timing requirements of the memory module."

Claim 32 of the present application recites the following: "The method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include an operational code selected from a set of defined operations codes and a set of associated parameters." These limitations are covered in claim 3 of the U.S. Patent – see above. (associated parameters- i.e. clock domain)

Claim 34 of the present application recites the following: "The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters." These limitations are covered in claim 4 of the U.S. Patent, which claims "The system of claim 3, wherein when invoked the command controllers issue the memory operations to the memory interface by sequencing through address ranges defined by the respective commands."

Claim 34 of the present application recites the following: "The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters." These limitations are covered in claims 15-17 of the U.S. Patent, which claim: 15. "The system of claim 1, wherein the commands conform to a generalized command protocol that substantially defines the test algorithm without regard to physical characteristics and timing requirements of the memory module." And 16. "The system of claim 15, wherein the command protocol defines a command syntax having a set of supported commands, and each command includes an operand and a set of parameters." And "17. The system of claim 16, wherein at least one of the commands includes fields to specify an address range, one or more memory operations to apply over the address range, and a bit pattern for application to the memory module of the address range." (a range can be a single address)

Claim 36 of the present application recites the following: "The method of claim 32, wherein the set of defined operation codes includes an operational code that directs

the sequencers to test a particular one of the memory modules." These limitations are covered in claim 1 of the U.S. Patent, which claims in part "...each sequencer controls the application of the test algorithm to the respective subset of memory modules..." (a subset can contain a single element)

Claims 1, 23, 26, 28, 29, and 38 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 20 of U.S. Patent No. 7,184,915. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

The limitations of each of the independent claims 1, 26, and 28 of the present application are discussed above with respect to claim 1 of the U.S. Patent. Claim 20 of the U.S. Patent contains the limitations of claim 1 and further limitations as shown:

Claim 20 of the U.S. Patent claims "A system comprising: a plurality of memory modules, at least one of the memory modules having physical characteristics different than other of said plurality of memory modules, a single built-in self test WISP controller that stores a set of commands defining an algorithm for testing the plurality of memory modules; a plurality of sequencers, each sequencer associated with a respective set of one or more memory modules that share common physical characteristics and operative to receive the commands and issue one or more memory operations in accordance with the commands; and a plurality of memory interfaces, each memory interface operative to apply the memory operations to an associated memory module in accordance with physical characteristics of the memory module, wherein the BIST controller comprises: an algorithm memory that stores the set of commands as one of a

set of selectable memory test algorithms having associated commands; and an algorithm controller to retrieve the commands from the algorithm memory and issue the commands associated with the selected memory test algorithm to the sequencer, wherein the algorithm controller issues each of the commands to the sequencers in parallel for application to the respective subsets of the memory interfaces."

These limitations are covered in claim 20 of the U.S. Patent listed above. Claim 32 of the present application recites the following:" The system of claim 1, wherein BIST controller issues the commands to the sequencers in parallel for application to the memory modules."

Claim 38 of the present application recites the following:" The method of claim 29, wherein issuing an algorithm comprises issuing the commands to the sequencers in parallel for application to the memory modules."

Allowable Subject Matter

Claims 4-21, 30-31, 33, 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The limitation "...wherein each of the generalized commands includes a sequencer identifier that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules." cited in claim 4

of the present application along with the limitations of the independent claim 1 would render the claim allowable.

The limitation "...wherein directing application of the algorithm comprises issuing each of the commands to include a sequencer identifier that identifies one or more of the sequencers to process the command and apply the command to the respective memory modules." cited in claim 30 of the present application along with the limitations of the independent claim 28 would render the claim allowable.

The limitation "...wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation." cited in claim 33 of the present application along with the limitations of the independent claim 28 and claim 32 would render the claim allowable.

Claims 5- 21 are dependent either directly or indirectly on claim 4, therefore this combination would also cause the dependent claims to be allowable.

Claim 31 is dependent on claim 30; therefore, this combination would also cause the dependent claim to be allowable.

Claim 37 is dependent on claim 30; therefore, this combination would also cause the dependent claim to be allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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